February 22, 1999 *GFK-1200H*

Additions to the FBC User's Manual

Please retain this information with your *Bus Controller User's Manual* (GFK-1038A). A user manual is not shipped with the bus controller. User manuals can be ordered separately. They are also included in the document library on CD-ROM.

Capacities and Performance of this Release of the FIP Bus Controller

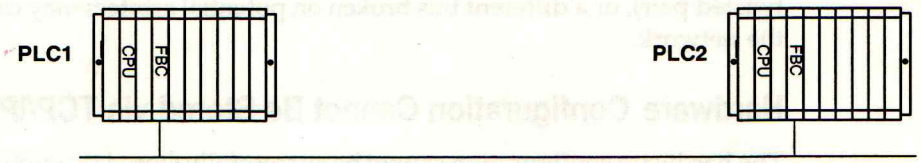
The information that follows provides a known benchmark for future regression testing. It also can be used to estimate the performance of a planned system.

This information is from actual measurements taken on a fully operational PLC and FIP network. The I/O data consisted of state TVAs only. Validator TVAs were not configured for exchange on the network. To achieve the best possible network performance, the elimination of validator TVAs is recommended.

Example 1

In this example, two PLCs (PLC1 and PLC2) are connected to a FIP network as shown below. PLC1 and PLC2 are configured with 4 synchronous scan sets at periods of 20ms, 40ms, 80ms, and 160ms. The logic of the sync programs in PLC1 increments a value and sends it to the corresponding sync program in PLC2. The logic of each sync program in PLC2 simply echoes the data it receives.

By increasing the length of the logic in a sync program in PLC1 to the point where the PLC becomes out of sync, a measurement can be made of the maximum amount of logic solution time available for that sync program. The measurements for the example system are shown in the following table. The measurements were taken by increasing the logic solution time of the 20ms logic to a point just before the program becomes synchronized. Leaving the 20ms program at that setting, another measurement was taken in the same fashion for the 40ms sync program. This method continued through the remaining scan sets.



PLC Configuration	Scan Sets	I/O (bytes)	Logic	Total logic
CPU925 FBC70 Sweep Mode: Microcycle Microcycle Period: 20ms Comm Window: 3ms 4 synchronous scan sets	Sync#1 @ 20ms	Input: 1 byte (1 TVA) Output: 1 byte (1 TVA)	7ms	56ms/160ms for 8 executions of the 20ms application
	Sync#2 @ 40ms	Input: 1 byte (1 TVA) Output: 1 byte (1 TVA)	9ms	36ms/160ms for 4 executions of the 40ms application
	Sync#3 @ 80ms	Input: 1 byte (1 TVA) Output: 1 byte (1 TVA)	6ms	12ms/160ms for 2 executions of the 80ms application
	Sync#4 @ 160ms	Input: 1 byte (1 TVA) Output: 1 byte (1 TVA)	7ms	7ms/160ms for 1 execution of the 160ms application
Total				111ms/160ms = 70% CPU available for logic solution