The table below breaks down the 20ms sync program into the different components of the microcycle. These components are explained in Chapter 4 of the *FIP Bus Controller User's Manual*.

The breakdown measures the data as it travels from the FIP network, passes through the FBC, and continues to the PLC application program. The breakdown continues as the data leaves the PLC application program, passes through the FBC, and returns to the FIP network.

Microcycle Scan Component	20ms sync scan Input: 1 byte (1 TVA) Output: 1 byte (1 TVA)
FBC Cons Delay	1ms Fixed
FBC Input	1ms
CPU Delay (3ms Comm window)	5ms Fixed (2ms + 3ms window time)
CPU Input	1ms
Available for logic	7ms
CPU Output	1ms
FBC Output	1ms
FBC Prod Delay	3ms Fixed
Total	20ms