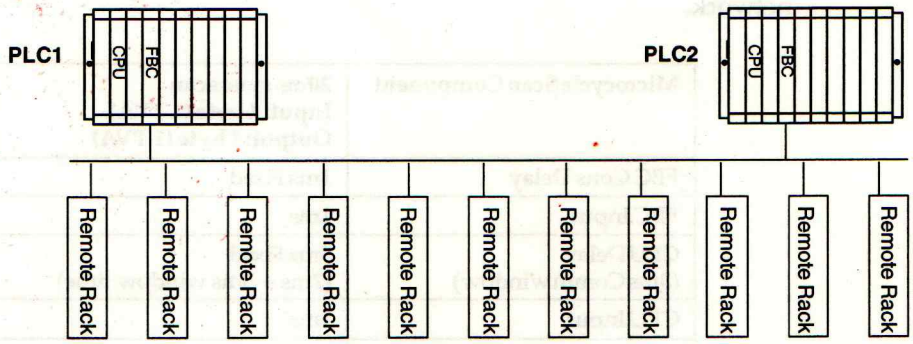
Example 2

In this example, 11 remote I/O racks are added to the two-PLC network described in example 1. Each remote I/O rack has an identical assortment of 19 I/O modules; ALG222 (5), ALG392 (6), MDL753 (3), MDL655 (5). This configuration uses two sync programs at periods of 100ms and 300ms.



CPU utilization is much higher in this example. This is mainly because there are fewer I/O scan operations between the CPU and the FBC during the same unit of time. With fewer I/O scan operations, more time is available for logic solution in the PLC CPU.

PLC Configuration	Scan Sets	I/O (bytes)	Logic	Total logic
CPU925 FBC70 Sweep Mode: Microcycle Microcycle Period: 100ms Comm Window: 10ms 2 synchronous scan sets	Sync#1 @ 100ms	Discrete Input: 220 bytes (55 TVAs) Discrete Output: 132 bytes (33 TVAs) Analog Input: 352 bytes (11 TVAs) Analog Output: 176 bytes (11 TVAs)	45ms	156ms/300ms for 3 executions of the 100ms application
	Sync#2 @ 300ms	Analog Input: 1408 bytes (44 TVAs) Analog Output: 880 bytes (55 TVAs)	126ms	126ms/300ms for 1 execution of the 300ms application
Total				261ms/300ms= 87% CPU available for logic solution

The table below breaks down the 100ms sync program into the different components of the microcycle. The breakdown measures the data as it travels from the FIP network, passes through the FBC, and continues to the PLC application program. The breakdown continues as the data leaves the PLC application program, passes through the FBC, and returns to the FIP network.

Microcycle Scan Component	100ms sync scan Input: 572 bytes (66 TVAs) Output: 308 bytes (44 TVAs)
FBC Cons Delay	1ms Fixed
FBC Input	23ms
CPU Delay (3ms Comm window)	5ms Fixed (2ms + 3ms window time)
CPU Input	2ms
Available for logic	52ms
CPU Output	2ms
FBC Output	12ms
FBC Prod Delay	3ms Fixed
Total	100ms